IN THE ABSTRACT

Please delete the current Abstract on Page 23 and replace with the following new Abstract:

A circuit includes a volatile memory array and a logic circuit operable to detect a memory array tamper situation and generate at least one control signal responsive thereto. Circuitry associated with each of the individual cells within the volatile memory array responds to the at least one control signal by destroying any data stored by the associated memory cell. Data is destroyed using one of several options including: shorting a true node of the latch to a complement node of the latch, shorting the true and complement nodes of the latch to a bit line and a complement bit line, shorting one of the true/complement nodes of the latch to a reference voltage, shorting both the true and complement nodes of the latch to at least one reference voltage, coupling a first and second positive reference voltage inputs to a positive/ground voltage supply, or shorting the bit line to a reference voltage while the pass gate is activated.